IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF ON BEHALF OF BRIAN K. CAMPBELL, ET AL.

PURSUANT TO 37 C.F.R. 41.31

APPLICANT:	Brian K. Campbell, et al.	*GROUP ART UNIT:*	2112
U.S.S.N.:	10/675,002	*CONFIRMATION NO.:*	**5206**
FILING DATE:	09/30/2003	*EXAMINER:*	**Alphonse, Fritz**
		CUSTOMER NO.	**24227**
TITLE:	*METHOD OF AND SYSTEM FOR ERROR CHECKING IN A DATA STORAGE SYSTEM*		

CERTIFICATE OF TRANSMISSION UNDER 37 C.F.R. §1.8(a)

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APPEAL BRIEF

This is an Appeal Brief in connection with an Appeal from a final rejection decision of the Primary Examiner dated October 1, 2007 in the above-identified application and pursuant to a Notice of Appeal filed on December 28, 2007. This Appeal Brief is being filed with a Petition for a Three Month Extension of Time pursuant to 37 C.F.R. 41.31 and 37 CFR 1.136.

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I. REAL PARTY IN INTEREST

The real party in interest is EMC Corporation, the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-20 are on appeal.

Claim 1 is rejected.

Claim 2 is rejected.

Claim 3 is rejected.

Claim 4 is rejected.

Claim 5 is rejected.

Claim 6 is rejected.

Claim 7 is rejected.

Claim 8 is rejected.

Claim 9 is rejected.

Claim 10 is rejected.

Claim 11 is rejected.

Claim 12 is rejected.

Claim 13 is rejected.

Claim 14 is canceled.

Claim 15 is rejected.

Claim 16 is rejected.

Claim 17 is rejected.

Claim 18 is rejected.

Claim 19 is rejected.

Claim 20 is rejected.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1

Independent claim 1 recites an error checking method comprising:

A. receiving a data element including parity information (Specification page 13, lines 5-8);

B. performing a parity check of the data element to determine whether the data element is valid (page 13, lines 21-23);

C. generating a CRC for the data element (page 13, lines 8-12 and 23-25); and

D. corrupting the generation of the CRC if the parity check performed determines that the data element is invalid page 14, lines 9-22).

Independent Claim 6

Independent claim 6 recites an error checking system comprising an input device for receiving a data element including parity information (Specification page 13, lines 6-8; element 602, Figs. 5 and 6); a parity check device for checking the parity information of the data element to determine whether the data element is valid (page 13, lines 8-10; element 622, Fig. 6); a CRC generator coupled to the parity check device for generating a CRC for the data element (page 13, lines 8-12 and 23-25; elements 624a, 624b); and an output device (page 14, lines 3-8; elements 634a, 634b) for transmitting the data element with the parity information and CRC to a downstream device over a transmission link (element M1). The parity check device (622) is operative to output a corruption signal to the CRC generator if the parity check device determines that the data element is invalid, to instruct the CRC generator to corrupt the CRC generation for that data element (page 14, lines 9-22).

Independent Claim 10

Independent claim 10 is directed to a data transmission system 610, Fig. 6, comprising a transmission device (Specification page 13, lines 4-5; page 14, lines 2-8; element 611a) for transmitting command data elements to a downstream device 220, Figs. 1, 2 and 4, the command data elements being generated and transmitted according to a predetermined protocol; and a reception device for receiving response data elements from the downstream device (page 15,

lines 23-24; element 611b), the reception device including a protocol checking device for checking at least one state of the response data elements to determine the validity of the at least one state of the response data elements (page 17, lines 1-21; element 682a, 682b).

Independent Claim 14

Independent claim 14 recites a data transmission system comprising a data transmission device for transmitting data elements to a downstream device (Specification page 13, lines 4-5; page 14, lines 2-8; element 611a) and a data reception device for receiving data elements from the downstream device (page 15, lines 23-24; element 611b). The data reception device includes an input CRC checking device coupled to receive the data elements from the downstream device for checking the validity of received data elements based on a CRC associated with each received data element (page 19, lines 23-28; elements 720a, 720b, Fig. 7); a memory device coupled to the input CRC checking device for storing data elements received from the downstream device after the data elements have been processed by the input CRC checking device (page 16, lines 7-8, page 19, lines 29-30, elements 664a, 664b); and an output CRC checking device coupled to receive the data elements from the memory device for checking the validity of the data elements based on the CRC associated with each data element (page 16, lines 20-26; element 680, Fig. 7).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claim 10 is anticipated by Hagiawara (U.S. Patent No. 5,450,419) under 35 U.S.C. §102(b); whether claims 1 and 6 are unpatentable under 35 U.S.C. §103(a) over Hagiawara in view of Parr (U.S. Pub. 2002/0194571); and whether claim 14 is unpatentable under 35 U.S.C. §103(a) over Hagiawara in view of Parr (U.S. Pub. 2002/0194571) and further in view of Hurt (U.S. Patent No. 6,954,885).

VII. ARGUMENT

REJECTION UNDER 35 U.S.C. §102(b)

Claim 10

Claim 10 stands rejected under 35 U.S.C. §102(b) as being anticipated by Hagiawara (U.S. Pat. No. 5,450,419). This rejection is appealed because Hagiawara does not teach every element recited in independent claim 10, as is required for a proper rejection under 35 U.S.C. §102.

Hagiawara teaches a ring transmission system including a main controller 2 and a plurality of error checking nodes 3-1 to 3-n. Communication data is transmitted from the main controller 2 to the nodes 3-1 to 3-n. The nodes check the communication data for errors in data length and in an associated CRC code. If errors are present, the node adds an error detection component to the communication data and returns the communication data, along with the appended error detection component, to the main controller. The original portion of the communication data, including the error correction codes, is not altered in any way.

Accordingly, Hagiawara does not teach "a transmission device for transmitting command data elements to a downstream device" and "a reception device for receiving response data elements from the downstream device" wherein "the reception device include[ing]es a protocol checking device for checking at least one state of the response data elements to determine the validity of the at least one state of the response data elements."

Specifically, Hagiawara does not teach a downstream device to which the transmission device transmits command data elements and from which the reception device receives response data elements. Further, each communication data transmitted by the main controller is the same communication data received by the nodes. Hagiawara does not teach "command data elements" and "response data elements."

Even if the nodes 3-1 to 3-n were to be considered downstream devices, then Hagiawara does not teach the recited reception device. Again, each communication data transmitted by the main controller is the same communication data received by the main controller, i.e., Hagiawara does not teach "command data elements" and "response data elements" as recited in independent claim 10 and described in the Specification.

Accordingly, Hagiawara does not teach or suggest every element recited in independent claim 10, as is required for a proper rejection under 35 U.S.C. §102.. Therefore, independent claim 10 is allowable over Hagiawara, and the rejection under 35 U.S.C. §102 should be withdrawn.

Claims 11-13 depend from independent claim 10 and are allowable for at least the same reasons as independent claim 10.

REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 1 and 6 were rejected under 35 U.S.C §103 (a) as being unpatentable over Hagiawara (U.S. Pat. No. 5,450,419) in view of Parr (U.S. Pub. 2002/0194571). This rejection is appealed because Hagiawara does not teach that which the examiner relies upon it to teach and, even if the references were combined, the combination does not teach the invention recited in either of independent claims 1 and 6.

Claim 1

Applicants respectfully assert that Hagiawara does not teach that which the examiner relies upon it to teach and, even if the references were combined, the combination does not teach the invention recited in either of independent claim 1.

As set forth above, Hagiawara teaches a ring transmission system including a main controller 2 and a plurality of error checking nodes 3-1 to 3-n. Communication data, including error correction codes, is transmitted from the main controller 2 to the nodes 3-1 to 3-n. The error correction codes enable the nodes to check the communication data for errors in data length and in an associated CRC code. If errors are present, the node adds an error detection component to the communication data and returns the communication data, along with the appended error detection component, to the main controller. The original portion of the communication data, including the error correction codes, is not altered in any way.

First, Hagiawara does not teach "receiving a data element including parity information." The communication data described in Hagiawara includes error checking codes ERC-1 and ERC-2, for enabling the nodes to determine if data length or CRC errors, respectively, are

present in the data. Hagiawara does not disclose that the received communication data includes parity information.

Second, Hagiawara does not teach "performing a parity check of the data element to determine whether the data element is valid." Hagiawara teaches using the CRC code ERC-2 for checking for CRC errors in CRC circuit 33. There is not teaching or suggestion of checking the parity of the communication data to determine its validity.

Third, Hagiawara does not teach "generating a CRC for the data element." As set forth in applicant's specification, in lines 10-12 of Page 13, CRC generation involves applying a checksum of the data that follows a particular formula. Hagiawara's CRC circuit 33 only checks for CRC errors in the communication data and his CRC error code addition circuit 39 adds a predetermined CRC error detection signal ERD-2 to the communication data. As shown in Fig. 5C, error detection signal ERD-2 includes a number of bits indicating the presence of a CRC error. No CRC codes are generated in either of these components.

Fourth, Hagiawara does not teach "corrupting the generation of the CRC if the parity check performed determines that the data element is invalid." As set forth above, Hagiawara does not teach checking the parity of the communication data. Therefore, he cannot teach doing *anything* based on the determination of such a check. Further, Hagiawara does not teach generating a CRC. Therefore, he cannot teach corrupting the generation of the CRC. As set forth above, upon detecting a CRC error, Hagiawara adds error detection code ERD-2 to the communication data. The original error check code ERC-2 is not altered in any way.

The examiner relies on Parr to make up for the fact that Hagiawara does not teach corrupting the CRC. Even if this combination was proper, and even if Parr taught what the examiner suggests it does, since Hagiawara does not teach *any* of the elements of independent claim 1, the addition of Parr would still not render claim 1 unpatentable over the combination.

Applicants assert that Parr also does not teach what the examiner suggests it teaches. Specifically, Parr does not teach corrupting the generation of a CRC. As specifically shown in Figs. 6 and 8, Parr generates a CRC mask prior to the transmission of data and removes the mask upon reception of the data. After performing a parity check (Step 76, Fig. 8), if the data is valid, it is accepted. If not, it is ignored. See Paragraph [0028], lines 24-25. Parr does not have a need to, and therefore does not teach, corrupting the CRC.

Accordingly, since Hagiawara does not teach *any* of the elements of independent claim 1 and Parr does not teach corrupting CRC, the combination of Hagiawara and Parr does not teach the invention recited in independent claim 1. Therefore, independent claim 1 is allowable over the combination and the rejection of claim 1 under 35 U.S.C. §103 should be withdrawn.

Claim 6

Applicants respectfully assert that Hagiawara does not teach that which the examiner relies upon it to teach and, even if the references were combined, the combination does not teach the invention recited in either of independent claim 6.

First, Hagiawara does not teach "an input device for receiving a data element including parity information." The communication data described in Hagiawara includes error checking codes ERC-1 and ERC-2, for enabling the nodes to determine if data length or CRC errors, respectively, are present in the data. Hagiawara does not disclose that the received communication data includes parity information.

Second, Hagiawara does not teach "a parity check device for checking the parity information of the data element to determine whether the data element is valid." Hagiawara teaches using the CRC code ERC-2 for checking for CRC errors in CRC circuit 33. There is not teaching or suggestion of checking the parity of the communication data to determine its validity.

Third, Hagiawara does not teach "a CRC generator coupled to the parity check device for generating a CRC for the data element." As set forth in applicant's specification, in lines 10-12 of Page 13, CRC generation involves applying a checksum of the data that follows a particular formula. Hagiawara's CRC circuit 33 only checks for CRC errors in the communication data and his CRC error code addition circuit 39 adds a predetermined CRC error detection signal ERD-2 to the communication data. As shown in Fig. 5C, error detection signal ERD-2 includes a number of bits indicating the presence of a CRC error. No CRC codes are generated in either of these components.

Fourth, Hagiawara does not teach "an output device for transmitting the data element with the parity information and CRC to a downstream device over a transmission link." As set forth above, Hagiawara only teaches communication data having a CRC code ERC-2. Hagiawara does not teach parity in addition to the CRC code ERC-2.

Fifth, Hagiawara does not teach that "the parity check device is operative to output a corruption signal to the CRC generator if the parity check device determines that the data element is invalid, to instruct the CRC generator to corrupt the CRC generation for that data element." As set forth above, Hagiawara does not teach checking the parity of the communication data. Therefore, he cannot teach doing *anything* based on the determination of such a check. Further, Hagiawara does not teach generating a CRC. Therefore, he cannot teach corrupting the generation of the CRC. As set forth above, upon detecting a CRC error, Hagiawara adds error detection code ERD-2 to the communication data. The original error check code ERC-2 is not altered in any way.

The examiner relies on Parr to make up for the fact that Hagiawara does not teach corrupting the CRC. Even if this combination was proper, and even if Parr taught what the examiner suggests it does, since Hagiawara does not teach *any* of the elements of independent claim 1, the addition of Parr would still not render claim 1 unpatentable over the combination.

Applicants assert that Parr also does not teach what the examiner suggests it teaches. Specifically, Parr does not teach corrupting the generation of a CRC. As specifically shown in Figs. 6 and 8, Parr generates a CRC mask prior to the transmission of data and removes the mask upon reception of the data. After performing a parity check (Step 76, Fig. 8), if the data is valid, it is accepted. If not, it is ignored. See Paragraph [0028], lines 24-25. Parr does not have a need to, and therefore does not teach, corrupting the CRC.

Accordingly, since Hagiawara does not teach *any* of the elements of independent claim 6 and Parr does not teach corrupting CRC, the combination of Hagiawara and Parr does not teach the invention recited in independent claim 6. Therefore, independent claim 6 is allowable over the combination and the rejection of claim 6 under 35 U.S.C. §103 should be withdrawn.

Claim 14

Independent Claim 14 was rejected under 35 U.S.C. §103 as being unpatentable over the Hagiawara (U.S. Pat. No. 5,450,419) in view of Parr (U.S. Pub. 2002/0194571) and further in view of Hurt (U.S. Pat. No. 6,954,885). This rejection is appealed because Hagiawara does not teach that which the examiner relies upon it to teach and, even if the references were combined, the combination does not teach the invention recited in independent claim 14.

Contrary to the examiner's assertions, Hagiawara's input circuit 30 is not an input CRC checking device. There is absolutely no disclosure in Hagiawara to suggest that CRC checking is done in input circuit 30. The only reference in Hagiawara to input circuit 30 is that "communication data from an upstream node is received by an input circuit 30 which decodes the data to an NRZ code when the input circuit 30 modulates and sends the data." (Col 3, lines 54-57). Accordingly, there is not teaching or suggestion that input circuit 30 is a CRC checking device.

Further, Hagiawara's output circuit 35 is not an output CRC checking device. There is absolutely no disclosure in Hagiawara to suggest that CRC checking is done in output circuit 35. As set forth in Column 4, lines 23-27, output circuit 35 simply receives signals output by switch 34. Accordingly, there is not teaching or suggestion that input circuit 30 is a CRC checking device.

Accordingly, Hagiawara does not teach what the examiner relies upon it to teach. Therefore, the combination of Hagiawara, Parr and Hurt suggested by the examiner is improper, because Hagiawara does not teach an input CRC checking device and an output CRC checking device for the memory device of Hurt to be coupled between. Accordingly, the combination cannot teach the invention recited in independent claim 14.

Therefore, since Hagiawara does not teach the input CRC checking device and an output CRC checking device of independent claim 14, the combination of Hagiawara and Hurt, even if proper, does not teach the invention recited in independent claim 14. Therefore, independent claim 14 is allowable over the combination and the rejection of claim 14 under 35 U.S.C. §103 should be withdrawn.

Claims 2-5 depend from independent claim 1 is allowable for at least the same reasons as independent claim 1; claims 7-9 depend from independent claim 6 and are allowable for at least the same reasons as independent claim 6; and claims 15 - 20 depend from independent claim 14 and are allowable for at least the same reasons as independent claim 14.

VIII. CLAIMS APPENDIX

1. An error checking method comprising:

A. receiving a data element including parity information;

B. performing a parity check of the data element to determine whether the data element is valid;

C. generating a CRC for the data element; and

D. corrupting the generation of the CRC if the parity check performed determines that the data element is invalid.

2. The error checking method of claim 1 further comprising transmitting the data element with the parity information and CRC to a downstream device over a transmission link.

3. The error checking method of claim 2 further comprising transmitting an alarm signal to the downstream device if the generation of the CRC has been corrupted in Step D.

4. The method of claim 1 wherein Step D comprises flipping a bit in an associated original CRC generated for a particular data element.

5. The method of claim 3 wherein, upon receiving the alarm signal, the downstream device resynchronizes the transmission link.

6. An error checking system comprising:

an input device for receiving a data element including parity information;

a parity check device for checking the parity information of the data element to determine whether the data element is valid;

a CRC generator coupled to the parity check device for generating a CRC for the data element; and

an output device for transmitting the data element with the parity information and CRC to a downstream device over a transmission link;

wherein the parity check device is operative to output a corruption signal to the CRC generator if the parity check device determines that the data element is invalid, to instruct the CRC generator to corrupt the CRC generation for that data element.

7. The error checking system of claim 6 further comprising an alarm device for transmitting an alarm signal to the downstream device when the CRC for a particular data element has been corrupted.

8. The error checking system of claim 6 wherein the CRC generator corrupts a CRC by flipping a bit of an associated original CRC generated for a particular data element.

9. The error checking system of claim 7 wherein the downstream device, upon receiving the alarm signal, resynchronizes the transmission link.

10. A data transmission system comprising:

a transmission device for transmitting command data elements to a downstream device, the command data elements being generated and transmitted according to a predetermined protocol; and

a reception device for receiving response data elements from the downstream device, the reception device including a protocol checking device for checking at least one state of the response data elements to determine the validity of the at least one state of the response data elements.

11. The system of claim 10 wherein the at least one state of the response data elements includes a data structure of the response data elements.

12. The system of claim 10 wherein, if the protocol checking device determines that the at least one state of the response data elements is invalid, it transmits a status signal to the transmission device to notify the transmission device of the invalidity.

13. The system of claim 12 wherein the status signal transmitted to the transmission device from the protocol checking device resets the transmission device.

14. A data transmission system comprising:

a data transmission device for transmitting data elements to a downstream device;

a data reception device for receiving data elements from the downstream device, the data reception device including:

an input CRC checking device coupled to receive the data elements from the downstream device for checking the validity of received data elements based on a CRC associated with each received data element;

a memory device coupled to the input CRC checking device for storing data elements received from the downstream device after the data elements have been processed by the input CRC checking device; and

an output CRC checking device coupled to receive the data elements from the memory device for checking the validity of the data elements based on the CRC associated with each data element.

15. The system of claim 14 wherein, if an invalid data element is detected by the input CRC checking device, the input CRC checking device notifies the data transmission device that at least one data element received by the data reception device is invalid.

16. The system of claim 15 wherein the memory device includes a First In-First Out (FIFO) memory device.

17. The system of claim 16 wherein the data reception device includes a first data element processing path and a second data element processing path for processing different portions of the received data elements.

18. The system of claim 17 wherein the input CRC checking device includes a first CRC checking unit coupled to the first data element processing path and a second CRC checking unit coupled to the second data element processing path.

19. The system of claim 18 wherein the FIFO memory device includes a first FIFO memory unit coupled to the first data element processing path for receiving data elements from the first CRC checking unit and a second FIFO memory unit coupled to the second data element processing path for receiving data elements from the second CRC checking unit.

20. The system of claim 19 wherein the first data element processing path processes the high bits of the received data elements and the second data element processing path processes the low bits of the received data elements.

IX. EVIDENCE APPENDIX

A. U.S. Patent No. 5,450,419 to Hagiawara

Cited by the examiner in the Office Action dated April 18, 2006.

B. U.S. Pub. 2002/0194571 to Parr

Cited by the examiner in the Office Action dated April 18, 2006.

C. U.S. Patent No. 6,954,885 to Hurt

Cited by the examiner in the Office Action dated April 18, 2006.

X. RELATED PROCEDINGS APPENDIX

None

XI. CONCLUSION

For the reasons set forth above, applicants respectfully assert that the rejections of claims 1-20 are unwarranted and improper and that the claims are allowable over the art of record. Accordingly, applicants respectfully request withdrawal of the rejections of claims 1-20.

Respectfully submitted,

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Date

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